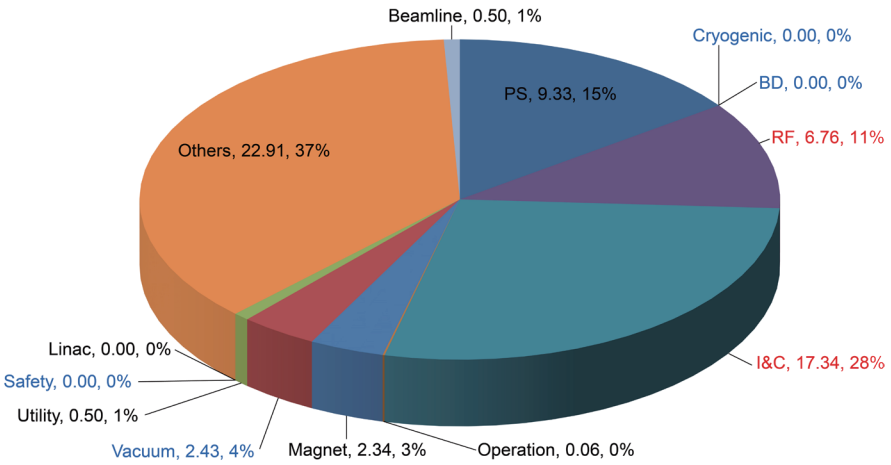

Fig. 7: Proportions of downtimes of the TPS accelerator in 2022. (62.17 hours in total)

Phase Drift Compensation Loop for a Radiation Frequency System of TPS Booster Ring

In synchrotron radiation light sources, the energies of electrons are provided by a radiation frequency (RF) system, which consumes substantial power. In 2015, members of the RF group worked to reduce this power consumption and develop an economic operation for RF systems in the Taiwan Light Source (TLS) booster ring.[1,2] In 2018, this economic operation system was implemented in the Taiwan Photon Source (TPS) booster ring.[3] The standard operation condition of the TPS is currently top-up mode operation with a 500-mA beam current of multiple bunches but with a single bunch of 3 mA in the middle of clear bunches (also known as hybrid-mode operation). Because of the high injection efficiency and long lifetime (over 8 h) during normal user operation, the injection period accounts for a small portion of the total time required to maintain a beam current fluctuation of less than 5 mA. Thus, the energy-saving operation is expected to reduce the power consumption of the booster ring considerably. Briefly, electron beams are injected from the booster ring to the storage ring to replenish the lost beam every 242 s. Thus, the booster ring operates only during the 2-s injection period and then rests for the remaining 240 s. At the beginning of the energy-saving operation for the TPS booster ring, only the magnets of the booster ring are powered off during the 240-s resting time. However, because the TPS booster RF system consumes 60 kW of electricity, the system should be operated in the power-saving mode.

Problem of Digital Low-Level RF During Economic Operation

Economic operation is realized using an energy-saving module, which controls the anode voltage and cathode current of the klystron to operate at a high level in the injection mode and at a low level in the standby mode. During switching between these two modes, the instant phase jump caused by the change in the klystron cathode current is beyond the compensation capacity of the digital low-level RF (DLLRF) system. Compared with an analog low-level RF system at the TLS or the TPS, the DLLRF control system has a wider bandwidth and a faster feedback response for improved feedback performance. Thus, the DLLRF control system can sense the aforementioned instant phase jump and consequently drive the proportional-integral-derivative (PID) controller to reach saturation rapidly and thereby trigger RF interlocking to protect the system. **Figure 1** (see next page) depicts the phase jump as a digital-to-analog converter (DAC) output phase. To maintain a constant gap voltage phase, which is depicted as an analog-to-digital converter (ADC) phase in **Fig. 1**, the DLLRF system must compensate for phase differences up to approximately ±85°, similar to the DAC phase behavior during mode switching. As displayed in **Fig. 2** (see next page), this phenomenon enables the RF trip to occur smoothly. In **Fig. 2**, t_1 is the preparation zone for the klystron to increase the cathode current (I_{cc}) for pulling the maximum power up by increasing the anode voltage, so as anode current (I-anode) raising, whereas t_2 represents the first ramp of the gap voltage, which fails in this case. This failure clearly occurs as a result of the oscillation of

the DLLRF phase control, which primarily occurs because of the large phase jump. At this point, the tuner phase signal, which is defined as $\theta_{Pf} - \theta_{Pt} + \theta_{offset}$ (normally 0°), reaches -15° and results in a misjudgment of the tuner-feedback loop. This phenomenon triggers interlocking after approximately 0.6 s, which is referred to as "Interlock," at t_4, which results in the stoppage of the feedback loop and causes the system to switch to the tuning mode for protection. Therefore, when the phase drift exceeds the integrated limit of the RF system and the DLLRF at t_2, the DLLRF system exhibits a phase-lock fault. Although the phase drift slightly decreases and the gap voltage successively increases and decreases at t_3, a misjudgment already occurs in advance at t_2 to stop the feedback loop. Thus, the RF system generates constant RF power, and the beam injection process fails thereafter.

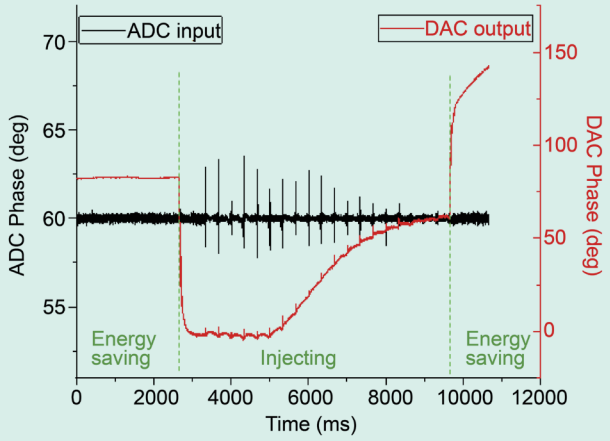

Fig. 1: Phase variations of the DLLRF system ADC input and DAC output during injection mode switching.

Phase Drift Compensation Loop

After several tests on and modifications to the DLLRF system,[4] we concluded that the optimal solution to eliminate the large phase drifts observed during switching between the energy-saving and injection modes is to implement a phase drift compensation loop (PDCL) in the DLLRF system to reduce the phase compensation load of the PID controller. As shown in **Fig. 3**, we relied on the principle of coordinate conversion to realize the PDCL logic. This logic is represented by the following three formulas:

$$\theta_0 = \theta_{PID_0} - \theta_{Pf_0} \quad \text{..... (1)}$$
$$\theta_1 = \theta_{PID_1} - \theta_{Pf_1} \quad \text{..... (2)}$$
$$\theta_2 = \theta_1 - \theta_0 \quad \text{..... (3)}$$

A coordinate rotation digital computer circuit was used to calculate the phases of the PID output, and P_f was calculated and sent to a subtractor to obtain the phase difference, as indicated by Eqs. (1) and (2). After the initial phase difference (θ_0) was obtained at a normal I_{cc} value, the instantaneous phase difference (θ_1) was calculated and subtracted from θ_0 to obtain the phase difference

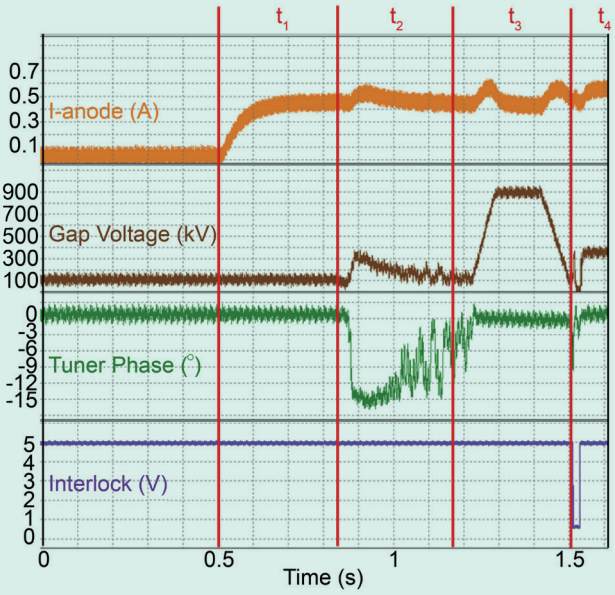

Fig. 2: Transient data of ramp gap voltage failure of the RF system in the TPS booster ring.

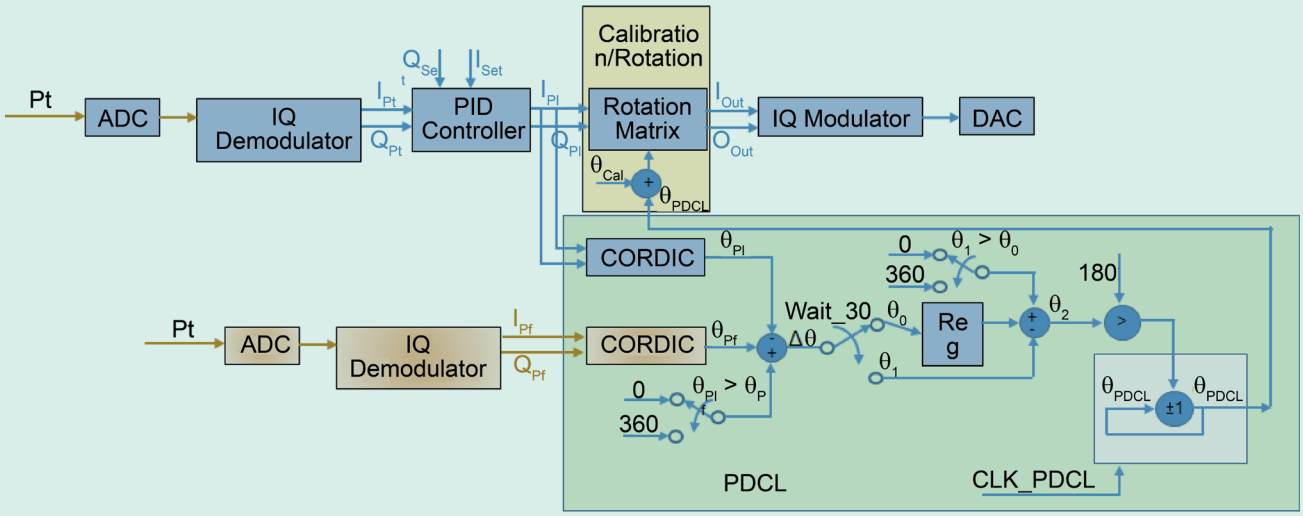

Fig. 3: Structure of the PDCL logic.

θ_2, as indicated by Eq. (3). The compensation direction was then determined to be counterclockwise when θ_2 was less than 180° and clockwise otherwise. Therefore, the compensation phase θ_{PDCL} was increased by 1° to approach the desired operation in the counterclockwise case, whereas this phase was decreased by 1° in the clockwise case. After θ_{PDCL} was obtained, it was then sent to a calibration/rotation circuit to calculate the output of the PID controller as new I_{out} and Q_{out} values. Finally, the output IQ data (the in-phase component and quadrature-phase component data) were modulated to an IF (intermediate frequency) band signal and then transmitted by the DAC to the klystron preamplifier to generate the expected RF power.

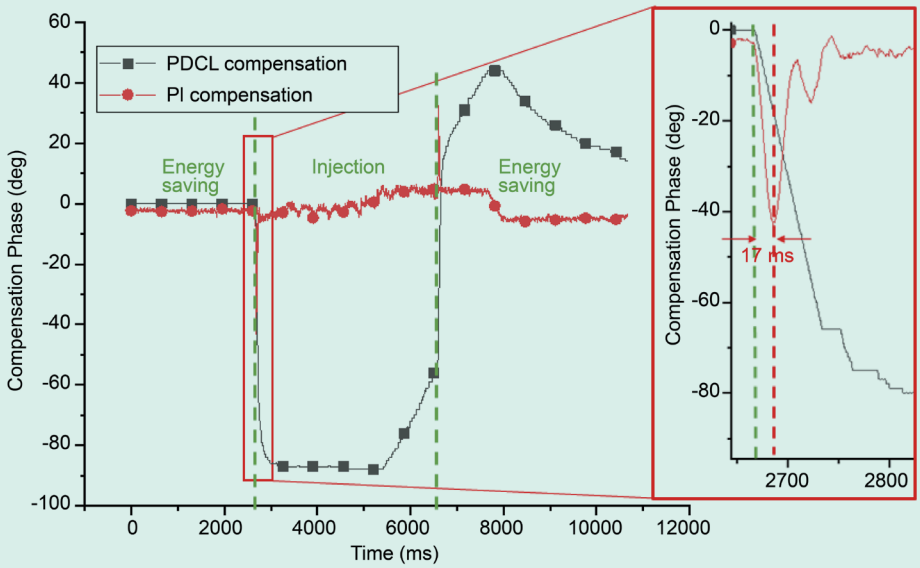

Fig. 4: Compensation phases of the PDCL and PID controller during mode switching.

Performance of the PDCL

Figure 4 depicts the phase compensation of the PDCL and PID controller during the entire injection period. The compensation provided by the PID controller and PDCL was 40° and 17°, respectively, during the first 17 ms of switching to the injection mode. The PDCL then mostly compensated for the phase drift to allow the PID controller to operate in an extremely limited loading range. Because the phase drift slope was considerably smaller than 1°/ms, the PID controller contributed to a rapid response to provide an immediate compensation of approximately -40° and 40° during switching to the injection mode and energy-saving mode, respectively. Simultaneously, the PDCL contributed to a slow but stable compensation phase with a constant speed of 1°/ms as expected. The combination of the PID controller and PDCL allowed the phase of the RF cavity to remain stable during the entire injection period.

Improvement of the Phase Accuracy

Figure 5 depicts the measured P_t phases with and without a PDCL in the DLLRF system for the TPS booster RF system. During the injection period, phase P_t remained stable within ±0.7° when the PDCL was used, whereas the set gap voltage of the cavity regularly fluctuated at a frequency of 3 Hz. This scenario was regarded as a considerable improvement to the ±3.5° fluctuation observed in the absence of a PDCL. The distribution of the phase errors of the two operating conditions was examined by counting the phase errors within various ranges while the gap voltage fluctuated.

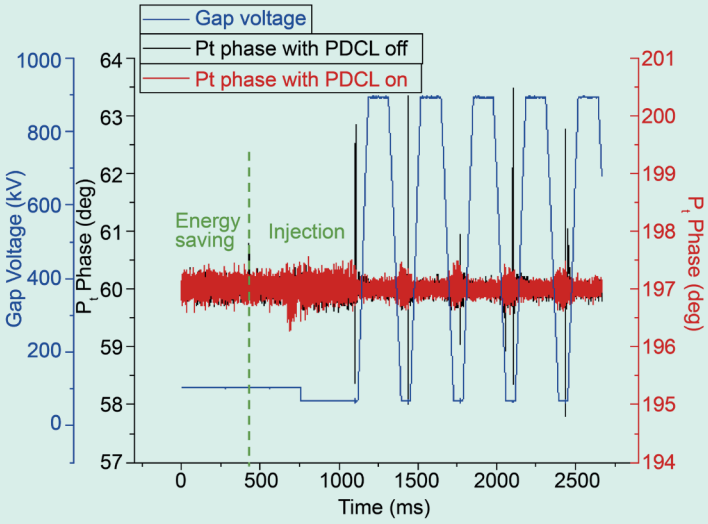

Fig. 5: Accuracy improvement achieved for the P_t phase by using the PDCL.

Power-Saving Ratio

Table 1 (see next page) presents the annual power consumption data under various conditions. Each normal injection cycle spanned 242 s, which comprised a standby period (240 s) and brief injection period (2 s). The annual power consumption values for the PDCL and no-power-saving scenario were 527.82 and 1324.32 MWh, respectively. The power-saving ratio (PSR) was calculated using the following equation:

$$PSR = \frac{P_{Energy\ saving\ off} - P_x}{P_{Energy\ saving\ off}} \times 100\% \quad \text{..... (4)}$$

where $P_{Energy\ saving\ off}$ is the annual power consumption in the no-power-saving scenario and P_x is the annual power consumption of the PDCL. In this scenario, the PDCL not only had a high PSR of 60% but also achieved stable gap voltage phase control. Therefore, the PDCL is the optimal

solution to achieve high stability and PSR. (Reported by Fu-Yu Chang, Zong-Kai Liu and Meng-Shu Yeh)

Table 1: Power consumption with the PDCL.

	With PDCL	Energy saving off
Standby I_{cc} (A)	1.81	4.90
Injection time (s)	2	2
Stand by time (s)	240	240
Cycle (s)	242	242
Standby power (kW)	61	--
Injection power (kW)	155	155
Power/cycle (kW s)	14,950	37,510
Power/year (kW h an^{-1})	527,821	1,324,320
PSR (%)	60.1	0.0

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Pulsed Wire System for Magnetic Field Measurements

A pulsed wire system was established for measuring the magnetic field of an in-vacuum undulator at the NSRRC in Taiwan.[1] A CuZr wire (length: 4 m, diameter: 100 μm) is used, and the pulse current is generated using an in-house power supply. A high-resolution, rapid-feedback laser-photodiode system is used to detect wire displacement. A NdFeB permanent magnet in-vacuum undulator (period: 22 mm, magnetic length: 2 m) was constructed for the Taiwan Photon Source (TPS). For this application, we employed a thin, highly stiff CuZr wire to reduce the maximum sag during the measurement of the long undulator. We compared the magnetic field measurements obtained with the pulsed wire with those obtained with a Hall probe.

Introduction

An in-vacuum undulator is a key insertion device for synchrotron radiation. The permanent magnet of the in-vacuum undulator is critical for the TPS at the NSRRC. Before installation in the storage ring, the magnetic fields of the undulators were measured during operational pauses. Typical methods for measurement of the magnetic fields of in-vacuum undulators use Hall probe and stretched wire measurements. In 1988, Warren first used a pulsed wire method to measure the integral field of a wiggler.[2] In addition to measuring the magnetic fields of undulators, pulsed wire measurements can be used for magnet alignment. In this study, we focused on the measurement of the magnetic field of a long undulator.

Pulsed Wire Measurement at the NSRRC

The theory of pulsed wire measurement is based on the Lorentz force and a general traveling wave. Short and long current pulses are used for first and second integral measurements, respectively. The wire displacement and can be written as[3]

$$U_{1st}(t) = \frac{IC_0\delta t}{2T}\int_0^{C_0 t} B_y(z)dz \quad \text{.....} \quad (1)$$

$$U_{2nd}(t) = \frac{I}{2T}\int_0^{C_0 t}\int_0^{C_0 t'} B_y(z)dzdz' \quad \text{.....} \quad (2)$$

where I is the magnitude of the current, δt is the current pulse width, T is the wire tension, and C_o is the wave velocity. **Figure 1** shows the pulsed wire system installed on an in-vacuum undulator, which contains a CuZr wire, an in-house power supply, two oil dampers, and a wire-displacement detection system.